What is claimed is:

1. A method of encoding at least one input bit set of N ordered bits with permutation position integers $I(k)$, where $k+1$ to N comprising the steps of:

a. encoding said input bit set using a first encoder having a multi-state register to provide a first output;

b. selectively reordering the input bit set using a hybrid S-random interleaver to provide a reordered input bit set, whereby said interleaver reorders said integers $I(k)$ such that once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L= 2^m-1$, n is a positive integer defined as $k-nL \geq 0$ and $nL \leq S$, and S is an arbitrary predetermined value; and

c. encoding said reordered input bit set using a second encoder having a multi-state register to provide a second output; whereby the value of said second encoder register is the same as the value of said first encoder register upon completion of step c.

2. The method of claim 1, further comprising the steps of:

generating a set of tail bits for each said input bit set; and

applying said tail bit set to reset the registers of both said first and second encoders.

3. The method of claim 1 wherein said selective reordering comprises the steps of:

a) receiving a plurality of N information bits where N is a positive integer;

b) defining the hybrid interleaver frame size N;

c) generating random integers $I(k)$ for k from 1 to N that satisfy the conditions:

1) $|I(k) - I(k-j)| > S$, where S is an arbitrary value and j is a positive integer, $0 < j \leq S$ and $k-j \geq 0$;

2) *If* $nL > S$, where L is dependent upon the number of encoder register states and n is a positive integer subject to $k - nL \geq 0$, then proceed to step 4;

3)$|I(k) - I(k-nL)| \neq jL$ where if not true, repeat steps 1-3;

4) verifying each random integer using $k \bmod 2^m - 1 = I(k) \bmod 2^m - 1$, where 2^m is the number of register states of one of said encoders, if not true, repeat steps 1-4; and

d) outputting permuted interleaver data sequence for encoding.

4. The method of claim 3 wherein step 4 further comprises incrementing the integer bit count k; and if $k \neq N + 1$, repeat steps 1-4.

5. The method of claim 2 further comprising the steps of:

a) acknowledging that encoding by said first and second encoder is complete;

b) switching inputs to said first and second encoder from an information bit stream and a permuted bit stream respectively to common feedback from said first constituent encoder last stage; and

c) incrementing the number of tail bits received from said feedback until said number of tail bits are greater than the number of registers used in said first constituent encoder, and if not, repeat steps b - c.

6. A transmission method, including encoding at least one input bit set of N ordered bits with permutation position integers $I(k)$ prior to transmission, where $k=1$ to N, comprising the steps of:

a. encoding said input bit set using a first encoder having a multi-state register to provide a first output;

b. selectively reordering the input bit set using a hybrid S-random interleaver to provide a reordered input bit set, whereby said interleaver reorders said integers $I(k)$ such that

once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L= 2^m-1$, n is a positive integer defined as $k-nL \geq 0$ and $nL \leq S$, and S is an arbitrary predetermined value; and

c. encoding said reordered input bit set using a second encoder having a multi-state register to provide a second output; whereby the value of said second encoder register is the same as the value of said first encoder register upon completion of step c.

7. The transmission method of claim 6, further comprising the steps of:

generating a set of tail bits for each said input bit set; and

applying said tail bit set to reset the registers of both said first and second encoders.

8. The transmission method of claim 5 wherein said selective reordering comprises the steps of:

a) receiving a plurality of N information bits where N is a positive integer;

b) defining the hybrid interleaver frame size N;

c) generating random integers $I(k)$ for k from 1 to N that satisfy the conditions:

1)$|I(k) - I(k-j)| > S$, where S is an arbitrary value and j is a positive integer, $0<j\leq S$ and $k-j\geq 0$;

2) *If* $nL > S$, where L is dependent upon the number of encoder register states and n is a positive integer subject to $k - nL \geq 0$, is not true, then proceed to step 4;

3)$|I(k) - I(k-nL)| \neq jL$ where if not true, repeat steps 1-3;

4) verifying each random integer using $k \bmod 2^m - 1 = I(k) \bmod 2^m - 1$, where 2^m is the number of register states of one of said encoders, if not true, repeat steps 1-4;

d) outputting permuted interleaver data sequence for encoding.

9. The transmission method of claim 8 whereby step 4 further comprises incrementing the integer bit count k; and if $k \neq N + 1$, repeating step (c).

10. The transmission method of claim 7 further comprising the steps of:

a) acknowledging that encoding by said first and second encoder is complete;

b) switching inputs to said first and second encoders from an information bit stream and a permuted bit stream respectively to common feedback from said first constituent encoder last stage; and

c) incrementing the number of tail bits received from said feedback until said number of tail bits are greater than the number of registers used in said first constituent encoder and, if not, repeat steps b - c.

11. A method of encoding, prior to transmission, an input bit set of N ordered bits with permutation position integers $I(k)$, where $k+1$ to N comprising the steps of:

a. encoding said input bit set using a first encoder having a register to provide a first output;

b. selectively reordering the input bit set using an interleaver to provide a reordered input bit set, whereby said interleaver reorders said integers $I(k)$ such that once reordered, the value for $|I(k) - I(k-nL)|$ is not evenly divisible by L, where $L= 2^m-1$, n is a positive integer defined as $k-nL \geq 0$ and $nL \leq S$, and S is an arbitrary predetermined value; and

c. encoding said reordered input bit set using a second encoder having a register to provide a second output; whereby the value of said second encoder register is the same as the value of said first encoder register upon completion of step c.